REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated October 6, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-7 are under consideration in this application. Claims 1 and 4-5 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention. New claims 6-7 are being added to recited other embodiments described in the specification.

Additional Amendments

The claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Prior Art Discussion

Claims 1 - 5 were rejected under 35 U.S.C. §102(e) on the grounds of being anticipated by US Pat. No. 6,678,645 to Rajsuman et al. (hereinafter "Rajsuman"). This rejection has been carefully considered, but is most respectfully traversed as follows.

The semiconductor integrated circuit device 60 of the invention, as now recited in claim 1 (e.g., Fig. 1), comprises: first and second circuit blocks 601, 602; an interface checker 70 which is installed on the semiconductor integrated circuit device ("*the interface checker for design data A can be installed on the hardware chip and the LSI 60 including the interface checker 70 can be provided*" p. 10, lines 22-25) and monitors whether waveforms of signals between the first and second circuit blocks 601, 602 conform to an interface specification of a design data of the first circuit block 601; and an external output pin 80 which outputs a result of a monitoring of the interface checker outside of the semiconductor integrated circuit device 60.

The invention as recited in claim 4 is directed to a design method of a semiconductor integrated circuit device 60 comprising: providing a design data and an interface specification of the design data; generating a synthesizable interface checker in accordance with the interface specification; producing a semiconductor integrated circuit device 60 including a first circuit block 601 according to the design data and the interface checker 70 according to the synthesizable interface checker; and using the interface checker 70 installed on the semiconductor integrated circuit device 60 to monitor whether waveforms of signals between the first circuit block 601 and another circuit block 602 conform to the interface specification of the design data.

As recited in the new claims 6-7, the interface checker 70 is also incorporated into the semiconductor integrated circuit device 60 for logic synthesis and verification. ("*making it possible to incorporate the interface checker into a fabricated system LSI*" p. 5, lines 11-12; "*the interface checker of the present invention can be incorporated into the LSI in contrast with the conventional interface checking block whose description focuses on only the efficiency of simulation and ignores logic synthesis for installing it on the LSI in order to enhance the efficiency of logic simulation*" p. 8, line 26- p. 9, line 3)

"*Because the interface checker has conventionally taken the simulation efficiency as important and ignored logic synthesis capability, it has been impossible to use the interface checker for a run model for a logic emulator that is specialized hardware. In the present invention, because the hardware description of the synthesizable interface checker can be synthesized, the interface checker can be incorporated into a run model for logic emulator and high-speed logic verification can be performed* (p. 11, lines 18-22)."

As such, the invention not only incorporates the interface checker 70 into the semiconductor integrated circuit device 60 for logic synthesis and verification during the design stage, but also install the interface checker 70 on the semiconductor integrated circuit device 60 to monitor waveforms conformation after the semiconductor integrated circuit device 60 is fabricated ("*an object of the present invention is to provide means for determining whether any functional block included in a system LSI has a design error or is used by incorrect usage in the event that the system LSI malfunctions after fabricated*" p. 4, lines 22-26)

Applicants respectfully contend that Rajsuman fails to teach or suggest such an "interface checker 70 incorporated into a semiconductor integrated circuit device 60 for logic

synthesis and verification during the design stage, and installed on the semiconductor integrated circuit device 60 to monitor waveforms conformation after the semiconductor integrated circuit device 60 is fabricated (during the actual use of the semiconductor device)" or "an external output pin outputting a result from the interface checker outsides of the semiconductor device" according to the invention.

In contrast, Rajsuman (Fig. 3) designs a SoC (system-on-a-chip) 3 having circuit blocks/cores A, B, C under an electronic design automation (EDA) environment 41 with use of CAD tools (col. 6, lines 45-51), and then coverts the design data 45 into physical level data for producing an actual SoC (col. 6, lines 60-67). "*Rather than directly testing the complete SoC, separate ICs representing individual cores in the SoC 43, such as cores A, B and C are utilized in the design validation station 50* (col. 6, last line – col. 7, lines)." Rajsuman (Fig. 5) then verifies each of the cores by placing individual cores 681-685 on design validation stations DVSs 50 and using an interconnect bus 71 of to transact the data between the individual cores (col. 10, line 52 - col. 11 line 3).

Firstl, Rajsuman only has ***external*** validation stations for testing each of the blocks/cores of the SoC, but not any interface checker ***installed on*** the semiconductor integrated circuit device SoC to monitor waveforms conformation of the whole SoC.

Second, Rajsuman actually teaches away form the invention by testing each of the blocks/cores of the SoC, rather than the whole SoC. It is well established that a rejection based on cited references having contradictory principles or principles that teach away from the invention is improper.

Third, the interface of each of Rajsuman's blocks/cores can only be physically verified by transactions anticipated during the test, rather than after the SoC is fabricated and in the actual usage. Rajsuman can verify each core "*to be integrated in the SoC* (Abstract, line 4)", but not after the SoC is fabricated.

Fourth, as Rajsuman does not disclose any interface checker fabricated on a semiconductor device, it does not teach any external output pin outputting a result from such an interface checker to the outside of the semiconductor device.

Lastly, as Rajsuman does not disclose any interface checker fabricated on a semiconductor device, it does not teach incorporating such an interface checker 70 into the semiconductor integrated circuit device 60 for logic synthesis and verification during the design stage as recited in claims 6-7. Rajsuman does not incorporate the design validation stations DVSs 50 into the SoC for logic synthesis and verification during the design stage.

Applicants contend that the cited prior art reference fails to teach or disclose each and every feature of the present invention as recited in independent claims 1 and 4. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference. Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

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